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Behavior Analysis of Omega Network Using Multi-Layer Multi-Stage Interconnection Network

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Abstract
This paper consists the study of Omega network, that how the buffer cost affects by adding the stages into the Omega network which is further known as Omega-I and Omega – II respectively. The study analyzes the behavior of Omega Network using Multi - Stage Interconnection Network and Multi - Layer Multi - Stage network.

Keywords**:** MINs (Multi Stage Interconnection Network), MLMINs (Multi Layer Multi Stage Interconnection Network), SEs (Switching Elements), Omega Network, Buffer Cost.

I. Introduction

Multistage Interconnection Networks plays a vital role on the performance of the multiprocessor system. The Multistage Interconnection Networks (MINs) are an important part of these systems that enable the processors (input) to communicate with themselves and with the memory modules (output). Multistage Interconnection Networks (MINs) are designed to provide fast and efficient communication at a reasonable cost. In general, MINs consist of layers of switching elements (SEs) with a specific topological pattern.

The number of stages, interconnection topology, and the type of SEs used in the network configuration differentiate each MINs fault tolerant. Examples of the widely used MINs include: Omega Network, Gamma Network, Extra-Stage Gamma network, Delta Network, Tandem–Banyan Network and Multilayer MINs. Due to the size of its SEs and uncomplicated configuration of Omegas shown in Fig. 1, it is one of the most commonly used MINs.

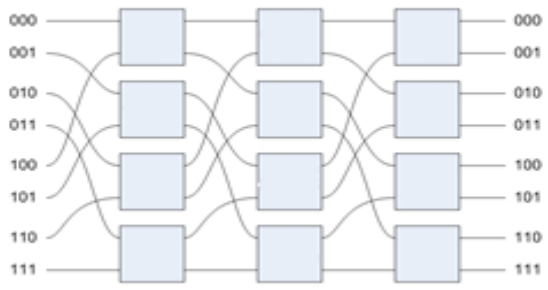

Figure 1: 8×8 Omega network

Architecture of MLMINs: The architecture of Multilayer Multistage Interconnection Networks presented in this paper is based on MINs with the Omega properties and on replicated MINs. The Omega is a unique-path MINs that has N input switches, N output switches and n stages, where n $=\log_2 N$. Each stage consists of N/2 interchange boxes, where each box being controlled individually through routing tags. An eight-input/eight-output Omega with three stages, 12 SEs and 32 links is shown in Figure 2. It is noted that there is only a single path between a particular input Si, i=1, 2, 3, 4, and a particular output D_i in the 8×8 Omega.

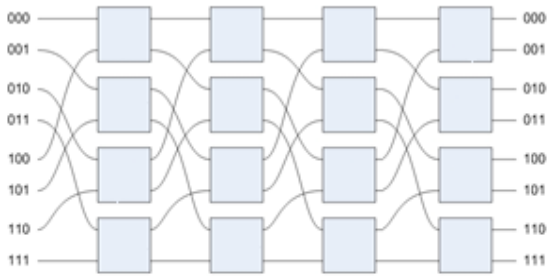

Figure 2: 8×8 Omega networks with extra-stage (OMEGA+1)

Omega+1 are a two-path derived from the omega by adding an extra-stage. Fig. 2 shows an eight-input/eight output Omega+1 with four stages consisting of 16 SEs and 40 links. Since the Omega+1 are a two-path MINs, there are two connection paths between a particular input and output. From the reliability point of view, this system can be represented as a parallel system path, consisting of $(\log_2 N)$-1 SEs each. Where, each path is connecting the input and output SE in series.

An 8×8 OMEGA+2 consists of eight inputs and eight outputs, four SEs per stage, five stages, and 48 links as demonstrated in Fig. 3.

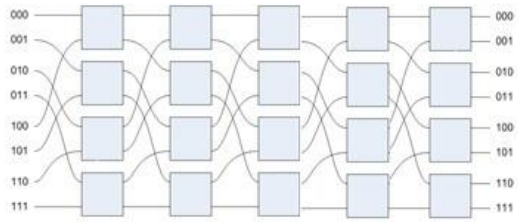

Figure 3: 8×8 Omega networks with additional stages (Omega+2)

Regular MIN: Multistage Interconnection Networks with the Omega property are networks where a unique path from an input to an output exists. Such MINs of size $N \times N$ consist of $c \times c$ switching elements with $n = \log_c N$ stages (Figure 4). That means it is a OMEGA network where all packets can use the same routing tag to reach a certain network output independently of the input at which they enter the networks. To achieve synchronously operating switches, the network is internally clocked. In each stage k ($0 \leq k \leq n$-1), there is a FIFO buffer of size $m_{max}(k)$ in front of each switch input. The packets are routed by store and forward routing or cut-through switching from a stage to its succeeding one by

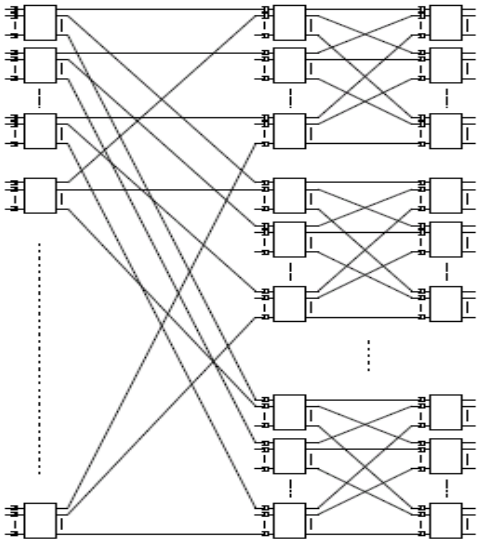

Figure 4: 3- stage Omega Network consisting c×c SEs

Back-pressure mechanism. Multicasting is performed by copying the packets within the $c \times c$ switches. In ATM context, this scheme is called cell replication while routing (CRWR). Figure 5 shows such a scenario for an 8×8 MINs consisting of 2×2 SEs. A packet is received by Input 3 and destined to Output 5 and Output 7.

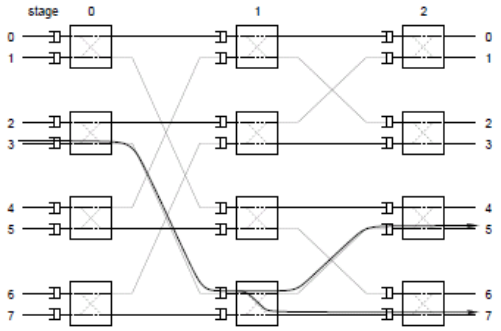

Figure 5: Multicasting while Routing

The packet enters the network and is not copied until it reaches the middle stage. Then, two copies of the packet proceed their way through the remaining stages. Packet replication before routing in the above example would copy the packet and send it twice into the network. Therefore, packet replication while routing reduces the amount of packets in the first stages. Comparing the packet density in the stages in case of replication while routing shows that the greater the stage number, the higher is the amount of packets.

Replicated MINs: It enlarge regular Multistage Interconnection Networks by replicating them L times. The resulting MINs are arranged in L layers. Corresponding input ports are connected as well as corresponding output ports. Figure 6 shows the architecture of an 8×8 replicated MINs consisting of two layers in a three-dimensional view.

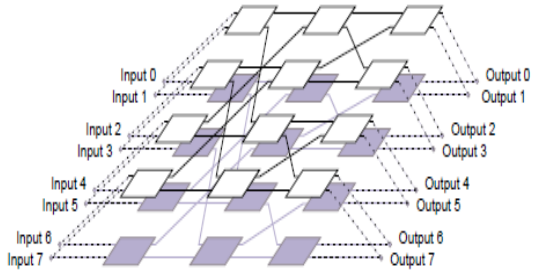

Figure 6: Replicated Multistage Interconnection Networks (L=2,3D view)

Packets are received by the inputs of the network and distributed to the layers. Layers may be chosen by random, by round robin, dependent on layer loads, or any other scheduling algorithm. The distribution is performed by a 1: L demultiplexer. At each network output, an L: 1 multiplexer collects the packets from the corresponding layer outputs and forwards them to the network output.

Two different output schemes are distinguished: single acceptance (SA) and multiple acceptances (MA). Single acceptance means that just

one packet is accepted by the network output per clock cycle. If there are packets in more than one corresponding layer output, one of them is chosen. All others are blocked at the last stage of their layer. The multiplexer decides according to its scheduling algorithm which packet to choose. Multiple acceptance means that more than one packet may be accepted by the network output per clock cycle. Either all packets are accepted or just an upper limit *R*. If an upper limit is given, *R* packets are chosen to be forwarded to the network output and all others are blocked at the last stage of their layer. As a result, single acceptance is a special case of multiple acceptances with $R = 1$.

In contrast to regular Multistage Interconnection Networks, replicated MINs may cause out of order packet sequences. sending packets belonging to the same connection to the same layer avoids destruction of packet order.

Multilayer MINs: Multilayer Multistage Interconnection Networks (MLMINs) consider the multicast traffic characteristics. As mentioned above, the amount of packets increases from stage to stage due to packet replication. Thus, more switching power is needed in the last stages compared to the first stages of networks. To supply the network with the required switching power, the new network structure presented in this paper replicates the number of layers in each stage. The factor with which the number of layers is increased is called growth factor *GF* ($G_F \in \mathbb{N} \setminus \{0\}$). Figure 7 shows an 8 × 8 MLMIN (3 stages) with growth factor $GF = 2$ in lateral view. That means the number of layers is doubled each stage and each switching element

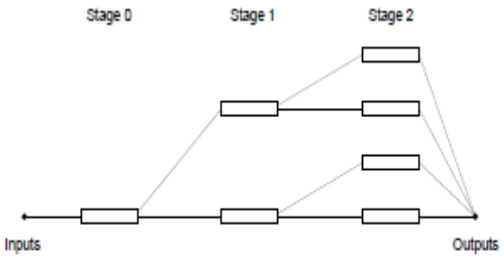

Figure 7: Multilayer Multistage Interconnection Network.(G_F=2)

Has twice as much outputs as inputs. Consider for instance that 2 × 2 SEs are used. Such architecture ensures that even in case of two broadcast packets at the inputs all packets can be sent to the outputs (if there is buffer space available at the succeeding stage). On the other hand, unnecessary layer replications in the first stages are avoided. Choosing $G_F = c$ ensures that no internal blocking occurs in an SE, even if all SE inputs broadcast their packets to all SE outputs.

To limit the number of layers and therefore the amount of hardware, two options are considered: starting the replication in a more rear stage and/or stopping further layer replication if a given number of layers is reached. The example presents an 8 × 8 MLMINs in which replication starts not before Stage 2 (last stage) with $G_F = 2$. A 3D view is given in Figure 8. The stage number in which replication starts is defined by $G_S (G_S \in \mathbb{N})$. Figures 4 and 5 introduce a MLMINs with $G_S = 2$. Of course, moving the start of layer replications some stages to the rear not just reduces the number of layers. It also reduces the network performance due to less SEs and therefore less paths through the network. It prevents exponential growth in case of large networks.

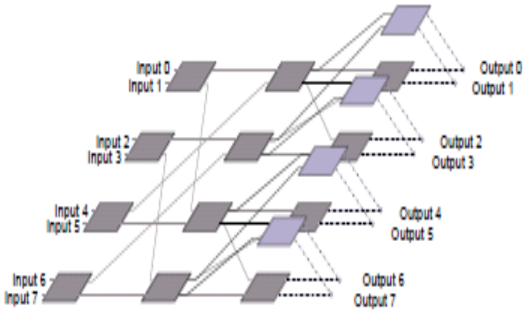

Figure 8: MLMINs in which replication start at stage 2(3D view)

II. Conclusion

The work in this paper is limited to study and experiment upto 2 stages of Omega Network in which the it is defined how the packets transformation speed is increased by replicating the stages of the network. In other words there are much more packets in the last stages due to replication than in the first stages. The only exception is if the traffic pattern results in such a destination distribution that packet replication has to take place at the first stage. Then, the amount of packets is equal in all stages.

III. Future Scope

An investigation of the influence of buffer size on the optimal number of network layers must be performed.

Dealing with various kinds of network traffic will also help to characterize MLMINs in more detail.

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